Claims

1. In a semiconductor random access memory product, a method of interleaving refresh operations with READ access cycles to effect interlaced asynchronous refresh of a DRAM array, the method comprising:

beginning a READ cycle in response to a predetermined input signal, the READ cycle comprising an array access period and a dataout period;

extending the duration of the array access period of the READ cycle by a predetermined refresh time slot; and

deferring commencement of the READ cycle access to the array until after the refresh time slot, so as to ensure adequate time for a pending refresh operation to complete before the READ cycle access to the array begins.

2. A method of interleaving refresh operations according to claim 1 wherein the READ cycle dataout period substantially immediately follows the array access period.

3. A method of interleaving refresh operations according to claim 1 wherein the refresh operation is a single-row refresh operation.

4. In a semiconductor random access memory product, a method of interleaving single-row refresh operations with WRITE access cycles to effect interlaced asynchronous refresh of a DRAM array, the method comprising:

beginning a WRITE cycle in response to a predetermined input signal, the WRITE cycle comprising a datain period and an array access period;

extending the duration of the array access period of the WRITE cycle by a predetermined refresh time slot; and

deferring commencement of the WRITE cycle access to the array until after the refresh time slot, so as to ensure adequate time for a pending refresh operation to complete before the WRITE cycle access to the array begins.

5. A method of interleaving refresh operations according to claim 4 wherein the WRITE cycle array access period substantially immediately follows the datain period.

6. A method of interleaving refresh operations according to claim 4 wherein the refresh operation is a single-row refresh operation.

7. A method of interleaving refresh operations according to claim 4 wherein the input signal comprises a write enable signal having a leading edge and a trailing edge, and said extending the duration of the array access period comprises inserting the refresh time slot in response to the trailing edge of the write enable signal.

8. In a semiconductor random access memory product, a method of interleaving single-row refresh operations with WRITE access cycles to effect interlaced asynchronous refresh of a DRAM array, the method comprising:

receiving a predetermined input signal signifying a WRITE access cycle; and

deferring internal execution of the WRITE operation until detecting a trailing edge of the said input signal, thereby eliminating a maximum write cycle time limitation.

9. A hidden refresh method of operating a DRAM array that implements external memory READ and WRITE access cycles, each READ access cycle comprising an array access period followed by a corresponding data out period, and each WRITE access cycle comprising a data in period followed by a corresponding array access period, the hidden refresh method comprising the steps of:

periodically generating a refresh request;

substantially immediately starting a refresh operation for at least one row of the DRAM array in response to the refresh request, unless a refresh start is currently prohibited;

detecting a leading edge of a predetermined input signal associated with a WRITE access cycle;

allowing a refresh start after detecting the leading edge of the input signal;

detecting a trailing edge of the input signal; and

prohibiting a refresh start after detecting the trailing edge of the input signal.

10. A hidden refresh method according to claim 9 wherein the input signal comprises a write enable signal.

11. A hidden refresh method according to claim 9 wherein the input signal comprises a select signal.

12. A hidden refresh method according to claim 9 wherein the leading edge of the input signal is a falling edge.

13. A hidden refresh method according to claim 9 and further comprising prohibiting a refresh start during the array access portion of a WRITE access cycle.

14. A hidden refresh method according to claim 9 and wherein said refresh time slot is inserted subsequent to a leading edge of the input signal.

15. A hidden refresh method according to claim 9 and wherein said refresh time slot is inserted subsequent to detecting an input data transition.

16. A hidden refresh method according to claim 15 wherein the refresh time slot has a duration T of at least a predetermined access time of the DRAM array.

17. A method according to claim 16 and further comprising, responsive to said prohibiting a refresh start, queuing the pending refresh request until the refresh start is no longer prohibited; and then starting the queued refresh operation.

18. A hidden refresh method of operating a DRAM array that implements external memory READ and WRITE access cycles, each READ access cycle comprising an array access period followed by a corresponding dataout period, and each WRITE access cycle comprising a datain period followed by a corresponding array access period, the hidden refresh method comprising the steps of:

periodically generating a refresh request;

substantially immediately starting a refresh operation for at least one row of the DRAM array in response to the refresh request, unless a refresh start is currently prohibited;

detecting a leading edge of a predetermined input signal associated with a WRITE access cycle;

detecting a trailing edge of the input signal; and

deferring the array access period corresponding to the WRITE access cycle until after the trailing edge of the input signal.

19. A hidden refresh method of operating a DRAM array that implements external memory READ and WRITE access cycles, each READ access cycle comprising an array access period followed by a corresponding data out period, and each WRITE access cycle comprising a data in period followed by a corresponding array access period, the hidden refresh method comprising the steps of:

periodically generating a refresh request;

substantially immediately starting a refresh operation for at least one row of the DRAM array in response to the refresh request, unless a refresh start is currently prohibited;

deferring commencement of a READ cycle access to the array until after a first predetermined time slot, to ensure adequate time for a pending refresh operation to complete before the READ cycle access to the array begins; and

prohibiting a refresh start during the array access portion of a READ access cycle but not during the data out period of the READ access cycle.

20. A hidden refresh method of operating a DRAM array according to claim 19 and further comprising, in a WRITE followed by READ sequence, overlapping the first time slot and the WRITE array access period.

21. A hidden refresh method of operating a DRAM array according to claim 19 and wherein the time slot T has a duration at least equal to a single-row refresh cycle array access time of the DRAM array.

22. A semiconductor random access memory product comprising:

A DRAM array; and

A DRAM controller circuit coupled to the array for implementing a hidden refresh feature, the controller circuit comprising:

a refresh generator circuit for generating refresh signals and refresh addresses;

an access arbiter circuit for inhibiting refresh operations at selected times; and

a single control signal path driven by the access arbiter circuit and coupled to the refresh generator circuit for controllably inhibiting/ allowing refresh signals to refresh the DRAM array.

23. A semiconductor random access memory product according to claim 22 wherein the refresh generator circuit includes an oscillator to provide a periodic refresh clock signal and a refresh address generator driven by the refresh clock signal to provide refresh addresses to the DRAM array.

24. A semiconductor random access memory product according to claim 22 wherein the refresh generator circuit includes:

an oscillator to provide a periodic refresh clock signal;

a refresh pulse generator to generate refresh pulse signals to the DRAM array; and

a FIFO memory coupled to receive the refresh clock signal for storing refresh requests as refresh request bits, the FIFO memory output coupled to the refresh pulse generator so as to trigger the generator to output a refresh pulse each time a refresh request bit is read from the FIFO memory; and wherein the single control signal path driven by the access arbiter circuit is coupled to a read enable input to the FIFO so that a refresh request bit is read from the FIFO memory only when allowed by the access arbiter single control signal.

25. In a semiconductor random access memory product, a method of interleaving refresh operations with READ access cycles to effect interlaced asynchronous refresh of a DRAM array, the method comprising:

beginning a READ cycle in response to a predetermined input signal, the READ cycle comprising an array access period and a dataout period;

deferring access to the array by inserting a predetermined refresh time slot;

deferring commencement of the READ cycle access to the array until after the refresh time slot, thereby ensuring time for a pending refresh operation to complete before the READ cycle access to the array begins; and

if the read cycle is prematurely terminated by a second address transition during array access, forcing a delay period prior to commencing a new read access cycle so as to allow the first READ access cycle to complete, thereby avoiding corruption of data stored in the DRAM array.

26. A method of interleaving refresh operations with READ access cycles according to claim 25 and further comprising extending the forced delay period beyond the read access time slot before prohibiting refresh start thereby allowing a refresh operation to start before beginning the new read access cycle.